REMARKS/ARGUMENTS

Claims 21, 24, 27, 28, 31, and 36 - 38 are pending.

Claims 21, 24, 27, 28, 31, and 36 - 38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Atchison, U.S. Patent No. 6,324,481 in view of Kirsch, U.S. Patent No. 6,507,933.

The present invention is directed to defect detection in a wafer inspection station. An aspect of the invention is the computation of probability metrics for defects which are located in specific regions (logic blocks) which comprise the logic circuitry of a semiconductor chip formed on a wafer. For example, independent claim 21 recites "position information of regions of a circuit pattern to be formed on said object [to be inspected]" and "a calculation device for ... calculating failure probabilities for said particles and said pattern defects positioned in said regions based on their sizes." Likewise, independent claim 36 recites "identifying positions and sizes of those of said particles or said pattern defects located in a region" and "calculating failure probabilities based on sizes of said pattern defects in said region."

It is earnestly submitted that Atchison et al. do not teach this aspect of the invention. Atchison et al. describe criteria for calculating "accurate yield results." Col. 5 lines 38 - 51. The criteria include inspection of a "sufficient number of wafers and lots of wafers." The inspections must be made at "critical steps" in the process line. Atchison et al. suggest that review of a "statistically significant number" defects should be made. These criteria do not teach "identifying positions [of] defects located in a region" and "calculating failure probabilities based on ... defects in said region."

Atchison et al. describe the notion of "critical area" for a given layer (e.g., metal 1). Col. 5, line 52 to col. 6, line 6. Critical area is defined as "the mathematical product of the die area ... times the probability of failure of the given type of failure." The probability of failure metric is obtained from "actual experience or from a computer simulation which uses the layout database for the layer in question." *Id* at lines 57 - 59. Atchison et al. then describe how a simulation can be performed to produce the probability of failure measure. The computation for

identifying the critical area and the simulations for obtaining the probability of failure measure do not teach Applicants' claim of "identifying positions [of] defects located in a region" and "calculating failure probabilities based on ... defects in said region."

Atchison et al. further disclose that the computation of the critical area "is repeated for different sizes of defects of interest, for example 1μ to 20μ, in 1μ increments." Col. 6, lines 7 - 14. Repeating the computation for different size defects does not show "identifying positions [of] defects located in a region" and "calculating failure probabilities based on ... defects in said region."

Atchison et al. next discuss calculating yield limits using the critical area concept, which requires quantitative data from the in-line defect inspection. Col. 6, lines 15 - 44. "The data that is generally required is actual defect densities (defects/unit area) by defect type and by layer." *Id* at lines 17 - 19. Atchison et al. describe computing defect density by defect type which "must take into account the number of defects reviewed or classified versus the total number of defects on the wafer. A random sample of the defects should be reviewed." *Id* at lines 21 - 23 (underlining added). Equation (1) represents a formula for computing defect density. Atchison et al. do not describe "identifying positions [of] defects located in a region" and "calculating failure probabilities based on ... defects in said region." In fact, they teach that a "random sample" of defects should be considered. This clearly does not teach, or suggest, the present invention.

Equations (2) and (3) are used to compute a defect size distribution for each type of defect. Col. 6, line 45 to col. 7, line 3. These equations do not involve "identifying positions [of] defects located in a region" and "calculating failure probabilities based on ... defects in said region."

Atchison et al. disclose a second method for calculating yield limits. Col. 7, lines 4 - 24. They discuss partitioning a wafer "into the blocks representing the individual die." *Id* at lines 9 - 10. In particular, "[o]ne way to calculate the killer probability is to eliminate die that have multiple defects and calculate killer probabilities for each defect type for those die having only one defect." *Id* at lines 11 - 13. The invention recites "identifying positions [of] defects located in a region" where a region is a block of logic of a circuit within a chip. By contrast,

Atchison et al. describe detail only to the die level; i.e., the wafer is partitioned into "blocks representing the individual die." This does not teach or suggest "defects located in a region" within the die. Moreover, Atchison et al. describe eliminating dice that have more than one defect, performing the probability computation for dice that have only one defect. This does not teach "calculating failure probabilities based on ... defects in said region" within a die.

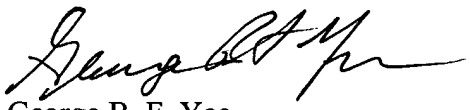
It is earnestly submitted that for any one of the foregoing reasons, the Section 103 rejection of the claims is believed to be overcome.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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